LUKE SUMMERS

Los Angeles, CA ▪ (714) 681-0581 ▪ lukesummers@ucla.edu

EDUCATION

Master of Science in Electrical and Computer Engineering | University of California, Los Angeles

Los Angeles, CA | Expected Graduation in Winter 2026

Coursework

- Advanced Computer Architecture, Linear Programming, Neural Signal Processing, Convex Optimization, Neural Networks and Deep Learning

Bachelor of Science in Computer Science | Harvey Mudd College

Claremont, CA | Overall GPA 3.6 | Major GPA 3.8 | Graduated with Distinction May 2025

Coursework

- **Computer Science:** Data Structures and Program Development, Computability and Logic, Computer Graphics, Computing Practices, Computer Systems, Algorithms, Real Time Systems
- **Math:** Linear Algebra, Single & Multivariate Calculus, Discrete Math, Statistics
- **Engineering:** Engineering Systems, Digital Electronics and Computer Engineering, Microprocessor Based Systems(class portfolio), System on Chip Design

Extracurricular Activities

- Claremont-Mudd-Scripps NCAA DIII Baseball Team

SKILLS

- **Programming/Hardware Description Languages:** C++, C, SystemVerilog, Python, R, Java, JavaScript
- **Protocols/Systems:** SPI, I2C, UART/USART, RTOS
- **Software/Hardware:** QuestaSim, KiCad, STM32, Lattice, Verilator, LTSpice, Gem5

EXPERIENCE

Software Engineer Intern — August 2024 – May 2025

SPADE | Claremont, CA

- Worked on multidisciplinary team conducting market research and developing a web application using Next.js, Node.js, and a python flask server
- Application displayed individual loan information for mortgage-backed securities and interacted with the Hedera distributed ledger to mint NFT's for each loan

Teaching Assistant — January 2023 – December 2024

Harvey Mudd College | Claremont, CA

- Graded homework assignments and led tutoring sessions for Intro to Computer Science, Computability and Logic, and Computer Systems courses

PROJECTS

Multi-class Classifier with Quantization — Fall 2025

- Multi-class classification implemented with linear and mixed integer linear programs solved with CVXPY
- Decentralized and centralized quantization done with LP and MILP solved with CVXPY
- Classification done for MNIST Fashion dataset

16 Bit FMA Module — Spring 2025

- Designed and verified a half precision floating point fused multiply-add unit for the OpenHW WALLY processor
- Focused on timing, correctness, and modular hardware design using systemverilog

Smart Chessboard(project website) — Fall 2024

- Co-designed an interactive mechatronic system that sense board state and provides real-time visual feedback for valid moves and check/check-mate conditions
- Developed on STM32L432KCUx MCU and UPduino v3.0 board with Lattice UltraPlus ICE40UP5K FPGA, integrating them with Hall effect sensors and LEDs